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09/638,194	08/11/2000	Sumio Koiwa	S004-4061	8149

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/638,194	KOIWA, SUMIO	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the Appeal Brief filed 6/26/3. In view of the arguments presented by Appellant in said Appeal Brief, the finality of Office Action of Paper No. 14 is herewith withdrawn. A new Final Rejection is herewith submitted. Please be referred to "Response to Arguments".

Response to Arguments

(A) Rejections under 35 USC 102(b) of claims 15-16 over Wen (Solid-State Electronics Volume 39 (9), pp. 1295-'8 (1996)):

(1) Counter to Appellant's allegation on page 6 of Appeal Brief, Wen et al do disclose a plurality of semiconductor layers in spaced-apart relation in a surface of the semiconductor layer. In Wen et al said plurality of semiconductor layers are is the pair of n+ layers (p. 1295, second column, and Figure 1), while in the Application said plurality of semiconductor layers is the pair of p+ layers 2a and 2b (cf. page 6 and Figure 1). The characterization of said plurality of semiconductor layers of Wen by Applicant as "ohmic contacts" (page 7, line 11 of second paragraph) fails to set said plurality apart from the plurality of semiconductor layers of Applicant, which also consists of a pair of diffusion layers in contact with metal (see Figure 1). Functionally and otherwise it is clear to one of ordinary skills in the art that the depletion layer 3 in Figure 1 of Applicant corresponds to the

(2) Counter to Appellant's allegation on page 7 of Appeal Brief, Wen et al do disclose a plurality of semiconductor layers disposed in spaced-apart relation in a surface of the semiconductor substrate (see Figure 1) while an interface level region of the surface of the semiconductor substrate because exactly the same procedure is followed by Wen et al (cf. p. 1296, first column, first five lines) as is described as the way to remove the interface level region by Applicant (see page 6, final paragraph). Therefore, there is as much and as little reason for Wen et al to disclose the absence of an interface level region as there is for Applicant.

(3) Counter to Applicant's allegation that the absence of an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, such absence does exist the wet etching used to implement the device necessarily influences the very upper monolayer surface of the semiconductor substrate, which is the only layer that can be said to reside between the plurality of (n+) semiconductor layers. Appellant is reminded that wet etching is the technique by which Applicant removes said interface level region according to the Specification (cf. page 8 of the original disclosure).

In summary on the rejections under 102(b) of claims 15-16 as being anticipated by Wen et al, I see no reason to withdraw the rejections.

(B) Rejection under 35 USC 103(a) of claims 1-7 as being unpatentable over Wen et al (loc. cit.) in view of APD (Admitted Prior Art):

Appellant substantially repeats the arguments of appeal of the rejections under 35 USC 102(b) discussed above, for which the same answers must therefore be given.

In addition, Appellant alleges that said standard photolithography and wet etching techniques are used to remove a portion in the area immediately above the n-type ZnSe layer (cf. page 13, final paragraph). However, said wet etching necessarily also influences the upper (monolayer) portion of said n-type ZnSe, which is the edged surface portion of the depletion layer disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, counter to the allegation of Appellant (cf. page 14).

Appellant's allegation that while the application teaches that the depletion layer surrounds the semiconductor layers (2a and 2b) and the examiner cited the Prior Art as Admitted by Applicant in this regard, "it is unclear how the examiner proposes to modify Wen et al in view of ADP so that the depletion layers surround the semiconductor layers..."; however, a specific proposition is included in the discussion on page 6: the distance between the semiconductor layers (n+ layers) can be decreased so as to merge the two depletion regions within the ZnSe layer. Alternatively, the voltage on cathode K can be increased if necessary so as to merge the two depletion regions within the ZnSe layer. This leaves no undepleted region adjacent said semiconductor layers at any angle. Motivation, to surround the said semiconductor layers, i.e., Wen et al aim to increase the sensitivity of the photodiode, from which point of view it does not make sense to leave any photosensitive area exposed to light undepleted.

On claim 2, a logical reasoning had been included in the argument by examiner and this logical reasoning is not traversed at all. While the examiner herewith withdraws

the rejection of claim 2 for not having replaced the official notice in a timely manner with an actual reference, such reference is readily available from the literature and provides adequate reason for rejection of claim 2 under 35 U.S.C. 103(a) as being unpatentable over Wen et al and Prior Art as Admitted by Applicant, and further in view of Chang Song Yin, as shown below.

In conclusion, the Final Rejection filed 1/1/33 (Paper No. 14) is herewith withdrawn. However, a new Final Rejection is herewith provided (see below).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 15-16*** are rejected under 35 U.S.C. 102(b) as being anticipated by Wen-Shiung Lour et al in Solid-State Electronics Volume 39, No. 9, pp. 1295-1298 (1996) (previously made of record to Applicant). *Wen-Shiung Lour et al teach* (cf. Fig. 1) a (PIN) photodiode comprising:

an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal (inherently for a photodiode, detection occurs through conversion of the optical incoming signal to an electric signal), the optical detection

portion having a semiconductor substrate of first conductivity type (P-Si) and an absorption layer consisting of i-ZnSe, also a semiconductor, thus together forming the equivalent of the "semiconductor substrate of first conductivity type" in the present invention (I-Zn-Se is p-type with negligible doping concentration); a plurality of (in fact: two) semiconductor layers of a second conductivity type (n-type here and indicated by "n+") formed in spaced-apart relation (i.e., spaced apart from each other) in a surface of the semiconductor substrate (surface marked to be 0.1 micron from the cathode K in Fig. 1).

Neither Wen-Shiung Lour et al nor the prior art description of Applicant referred to above specifically teach the non-existence of an interface level region of the surface of the semiconductor substrate in the area between the two semiconductor layers; however, this non-existence follows from the device specification: exactly the same procedure is followed by Wen-Shiung Lour et al as is described in the specification by Applicant, namely the removal by wet etching techniques to implement the device as depicted in Figure 1, so as to remove the interface level region (see Applicant's disclosure, page 6). Please note the absence of a semiconductor-semiconductor interface between the substrate and the region above its upper surface between the two semiconductor layers marked "n+". Although some defects may still exist near the upper surface due to asymmetry in the forces acting on the atoms near the surface and thus strict non-existence of interface levels can not be guaranteed (in fact, they never can be guaranteed to be wholly absent by virtue of the finite temperature at which the electrical device has to function if only because of the ohmic heating electric currents produce in

resistive media) this subtlety would equally apply to Applicant's invention: the device specifications in this regard are the same.

In conclusion, then, the limitation in claim 15 on the non-existence of an interface level region of the surface of the semiconductor substrate between the semiconductor layers, does not distinguish over Wen-Shiung Lour et al either, being inherent in the device as specified by Wen-Shiung Lour et al.

In conclusion, Wen-Shiung Lour et al anticipate claim 15.

With regard to claim 16: the first conductivity type (p-type) of the semiconductor substrate is different from the second conductivity type of the two semiconductor layers as taught by Wen-Shiung Lour (cf. Figure 1 and "Device Fabrication", column 2 on page 1295, lines 1-12). Therefore, Wen-Shiung Lour also anticipate claim 16.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-7*** are rejected under 35 U.S.C. 103(a) as being unpatentable over the international journal article by Wen-Shiung Lour et al in Solid-State Electronics Volume 39, No.9, pp. 1295-1298 (1996) (previously made of record and sent to Applicant), in view of Prior Art as Admitted by Applicant in his disclosure.

Wen-Shiung Lour et al teach (cf. Fig. 1) a (PIN) photodiode comprising:

an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal (inherently for a photodiode, detection occurs through conversion of the optical incoming signal to an electric signal), the optical detection portion having a semiconductor substrate of first conductivity type (P-Si) and an absorption layer consisting of i-ZnSe, also a semiconductor, thus together forming the equivalent of the "semiconductor substrate of first conductivity type" in the present invention (I-Zn-Se is p-type with negligible doping concentration); a plurality of (in fact: two) semiconductor layers of a second conductivity type (n-type here and indicated by "n+") formed in spaced-apart relation (i.e., spaced apart from each other) in a surface of the semiconductor substrate (surface marked to be 0.1 micron from the cathode K in Fig. 1) so that an etched surface portion of the semiconductor substrate is disposed between the semiconductor layers: see page 1296, first paragraph: the area between the said semiconductor layers has been etched away and the boundary between the portion that has been etched away and the absorption layer is the "etched surface portion" of Applicant. Moreover, whether or not the surface portion of the depletion layer is an etched surface portion or not is irrelevant to the present device claim.

While it is inherent to the operation of a photodiode that a depletion layer is formed in the semiconductor substrate by application of a reverse bias, *Wen-Shiung Lour et al do not necessarily teach* the further limitation that said depletion layer must *surround* the said semiconductor layers. However, a depletion layer that surrounds the said semiconductor layers with the specific advantage that the photosensitivity is improved (through a depleted area on the light-receiving surface) has been admitted to

exist in the prior art, as witnessed by Applicant's disclosure, particularly Figure 3 and pages 2 and 3. *Motivation* to include the teaching of the Prior Art as Admitted by Applicant in this regard into the device taught by Wen-Shiung Lour et al stems from the purpose of Wen-Shiung Lour et al to increase the sensitivity of the photodiode. Clearly, surface area between the said semiconductor layers not used as depletion region would detract from said purpose of Wen-Shiung Lour et al. The inventions can be easily *combined*, because all that is needed for the combination is a proper design of the distance between the said semiconductor layers in conjunction with the reverse bias. *Expectation of success* in implementing this combination is therefore *reasonable*.

Neither Wen-Shiung Lour et al nor the prior art description of Applicant referred to above specifically teach the non-existence of an interface level region of the surface of the semiconductor substrate in the area between the two semiconductor layers; however, this non-existence follows from the device specification: exactly the same procedure is followed by Wen-Shiung Lour et al as is described in the specification by Applicant, namely the removal by wet etching techniques to implement the device as depicted in Figure 1, so as to remove the interface level region (see Applicant's disclosure, page 6). Please note the absence of a semiconductor-semiconductor interface between the substrate and the region above its upper surface between the two semiconductor layers marked "n+". Although some defects may still exist near the upper surface due to asymmetry in the forces acting on the atoms near the surface and thus strict non-existence of interface levels can not be guaranteed (in fact, they never can be guaranteed to be wholly absent by virtue of the finite temperature at which the electrical

device has to function if only because of the ohmic heating electric currents produce in resistive media) this subtlety would equally apply to Applicant's invention: the device specifications in this regard are the same.

In conclusion, then, the further limitation newly introduced into claim 1, i.e., on the non-existence of an interface level region of the surface of the semiconductor substrate between the semiconductor layers, does not distinguish over Wen-Shiung Lour.

1. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wen-Shiung Lour et al and Prior Art as Admitted by Applicant as applied to claim 1 above, and further in view of Chang Song Yin (IEEE Electron Device Letters, Volume 12, No. 8, pp. 442-'3 (1991)). As detailed above claim 1 is unpatentable over Wen-Shiung Lour et al in view of Prior Art as Admitted by Applicant in his disclosure. However, it would have been obvious to include the teaching of claim 2 in the invention by Wen-Shiung Lour et al and Prior Art as Admitted by Applicant in view of Chang Song Yin, who teaches a highly responsive short-wavelength surface depletion layer photodiode with heavily doped semiconductor layers in a spaced-apart relation in a surface of a semiconductor layer (cf. Figure 1), -hence analogous art (cf. "Introduction", p. 442, first column), wherein the distance between neighboring heavily doped semiconductor layers (30 microns, see "Design of the Device", page 443, first column) is between half and two times the width of the depletion layer (cf. "Design of the Device", page 443, second column) for the entire range of the recommended depletion layer width (20 – 38 micron). Moreover, for reasons of efficiency the selection of the value of the "distance between

the second conductive type semiconductor layers formed on the surface of the first conductive type semiconductor region" as performed by one of ordinary skill in the arts must be between "0.5 to 2 times a width of the depletion layer in the horizontal direction formed by reverse biasing" (reverse biasing is the functional operational mode of photodiodes): if this distance were chosen to be less than half the width of the depletion layer there would be no net gain in having two separate second conductive type semiconductor regions and two electrodes. The cusp visible in Fig. 3 of the invention and cited as Prior Art would then be smoothed out, hence this Prior Art satisfies this part of the inequality. On the other hand, if the aforementioned distance were chosen to be greater than twice the depletion layer width the depletion layer would no longer be contiguous, resulting in a loss of photosensitivity because the first conductive type semiconductor region between the second conductive type semiconductor areas would be left unexploited. This would also be in contrast with the Prior Art shown in Fig. 3 of the present invention because this figure does show a contiguous depletion area. Finally, it is inherent in a photodiode of the type taught by the cited prior art that a reverse bias to the photodiode forms a depletion layer in the semiconductor substrate.

Therefore, it would have been obvious at least in view of Chang Song Yin to one of ordinary skills in the art to further specify the device taught by Wen-Shiung Lour et al so as to select the distance between the second conductive type semiconductor regions according to the further limitation formulated in claim 2.

With regard to claim 3: As detailed above, claim 1 (on which claim 3 depends) is unpatentable over the international journal article by Wen-Shiung Lour et al in view of

Prior Art as Admitted by Applicant. Furthermore, in their aforementioned journal article Wen-Shiung Lour et al specifically mention with regard to the device depicted in their Fig.1 that formed the basis of the above stated rejection of claim 1 that "standard photolithography and wet etching techniques are used to implement the device". See page 1296 of their article, first sentence. Therefore, the further limitation defined by claim 3 is taught by Wen-Shiung Lour et al. In conclusion, claim 3 does not distinguish over the prior art.

With regard to claims 4-7: claims 4-7 merely entertain the selection of either n- or p-type conductivities for the first and second type conductivities or conductive types in the invention as defined by claim 1. The examiner takes official notice that such selection is fully standard in the semiconductor device art and has therefore no patentable weight.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
August 14, 2003

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